W55MH32

Enhanced, True Random Number, Hardware Encryption Algorithm Unit, 32-bit MCU with 1024KB Flash, 10/100M Ethernet MAC and PHY, Hardware Internet controller with an integrated full TCP/IP stack, USB, CAN, 17 Timers, 3 ADCs, 2 DACs, Up to 12 communication interface

Features:

- Encapsulation
  - W55MH32L:100QFN(12x12mm)
  - W55MH32Q:68QFN(8x8mm)
- Core: 32-bit processor core
  - Up to 216MHz operation frequency,2.54DMips/MHz(CoreMark1.0)
  - Single-cycle multiplication and hardware division
- Memories
  - 1024K bytes of Flash memory
  - 96Kbytes of SRAM
- Clock, reset and supply management
  - 2.0～3.6V application supply and I/Os
  - POR, PDR, and programmable voltage detector (PVD)
  - 4～16MHz crystal oscillator
  - Internal 8MHz factory-trimmed RC
  - Internal 40kHz RC oscillator with calibration
  - 32kHz RTC oscillator with calibration
- Low-power
  - Sleep, Stop and Standby modes
  - supply for RTC and backup registers
- 3 x 12-bit, 1 μs A/D converters (up to 12 channels)
  - Conversion range: 0 to 3.6V
  - Temperature sensor
- 2 x 12-bit D/A converters
- DMA: 12-channel DMA controller
- Ethernet: 10/100M Ethernet MAC and PHY
  - Supports following Hardwired TCP/IP Protocols : TCP, UDP, ICMP, IPv4, ARP, IGMP, PPPoE
  - Supports 8 independent sockets simultaneously
  - Internal 32Kbytes Memory for Tx/Rx Buffers
  - 10BaseT/100BaseTX Ethernet PHY embedded
  - Support Auto Negotiation (Full and half duplex, 10 and 100-based)
  - LED outputs (Full/Half duplex, Link, Speed, Active)
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Embedded Tracking Module(ETM)
- I/O ports
  - 66(W55MH32L) / 36(W55MH32Q) multi-function bidirectional I/O ports, all mappable on 16 external interrupts
  - All GPIOs can be forced to configure pull-up and pull-down resistors
- Enhanced CRC calculation unit
- 17 Timers
  - 10 x 16-bit timers, each with up to 4 input
  - capture/output compare/PWM or pulse counter
  - and quadrature (incremental) encoder input
  - 2 x 16-bit, advanced motor control PWM timer with dead-time generation and emergency stop
  - 2 watchdog timers (Independent and Window)
  - SysTick timer 24-bit downcounter
  - 2 x 16-bit base timers
- Up to 12 communication interface
  - Up to 2 x I2C interfaces(support SMBus/PMBus)
  - Up to 5(W55MH32L) / 4(W55MH32Q) x USARTs
  - Up to 2 x SPIs, 1 multiplexed with I2S interface(only W55MH32L)
  - CAN interface(2.0B Active)
  - USB 2.0 full-speed interface(Optional internal
  - 1.5K pull-up resistor)
  - SDIO interface(only W55MH32L)
- Hardware encryption algorithm unit
  - Built-in hardware algorithm(DES、AES、SHA)
  - Provide a complete high-performance algorithm library
- TRNG: generate sequence of true random numbers
  - Four independent true random sources, which can be configured individually
  - 128bit random numbers can be generated at one time
  - Optional digital post-processing function
  - Attack detection
- SENSOR: voltage & temperature sensor alarm
  - VBAT and VDD voltage can be detected independently
  - Provide temperature detection sensor
  - Optional reset or interrupt after alarm
- SRAM scrambling
  - Support address and data scrambling
- One Time Programmable (OTP)
  - Support 32 Byte

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